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CHARACTERIZATION AND DESIGN OF GaAs MESFETs FOR BROADBAND CONTROL APPLICATIONS

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Abstract

A variety of discrete and monolithically integrated GaAs MESFETs have been characterized for microwave switching figure-of-merit and power handling capability. Design principles for GaAs FETs in broadband switching applications are presented with an emphasis on tradeoffs between conducting-state resistance, non-conducting state capacitance and power handling. Switching frequency figure-of-merit values between 200 and 400 GHz have been achieved with 1 watt power handling capability.

Introduction

GaAs MESFETs are becoming accepted as control devices for applications such as switching and phase shifting, particularly in monolithic circuit implementations. There have been some major contributions specifying relationships between device parameters and low power switching figure-of-merit,(1-3) although there has not been appreciable data presented on the dependence of control FET performance on device parameters. In addition, there has not been a focus on the tradeoffs between device and performance parameters for broadband circuit applications.

The purpose of this paper is to present an approximate switching figure-of-merit for broadband control applications which is useful for design and characterization, present low power and power handling data on a variety of discrete and monolithic MESFETs (different gate length, gate periphery, channel doping concentration and pinch-off voltage) and discuss device design aspects of GaAs MESFETs for control applications. Since FET switches have low bias consumption, have switching times of ~1nS and are capable of broadband design (bias port inherently isolated), optimization of switching and power handling will permit performance comparison with conventional circuits using silicon PIN diodes.

Control Device Characterization

Our approach to obtain a switching Q appropriate for broadband applications is depicted in Figure 1.(2,3) Since the impedance level for broadband switching applications is usually 50 ohms and the equivalent non-conducting state series resistance R_{NC} is less than R_C, we obtain an approximate switching Q of $\frac{1}{wC_{NC}R_C}$ or switching frequency figure-of-merit of $\frac{1}{2\pi C_{NC}R_C}$

In this program we characterized unpackaged chip devices in a SPST series switch (some tests with shunt mounting) from 50 MHz to 18 GHz. The gate is terminated in a 5K resistor to present a high RF impedance at all frequencies. Values of C_{NC} and R_C obtained from insertion loss and return loss measurements agreed well with the performance of more complicated control components using similar devices.

The power handling capability of a FET switch is dependent upon RF channel resistance if $V_{RF} > \frac{(V_{brG} - V_p)}{2}$ in the non-conducting state, where the RF current and voltage are peak values.(1) The SPST series switch configuration was tested at increasing CW power levels at 5 GHz in both conducting and non-conducting states. Since we do not have extensive correlation with similar devices used in control components under power handling conditions and have not correlated these results with DC gate breakdown tests, we report the broadband SPST switch CW power handling (or the line voltage and line current handling) results directly.

MESFET Parameter and Control Component Performance

Six sets of devices were measured, with gate lengths varying from 0.3 to 1.0μm, gate periphery 400 to 1200μm, and pinch off voltage from 2 to 6 volts. Both discrete FETs fabricated with vapor phase epitaxial channels and monolithic FETs fabricated with ion implanted channels were tested, although we have more extensive characterization of the epitaxial devices at this time. Although the FETs have device parameters typical of low noise, signal or power devices, particular emphasis was placed on evaluation of high pinch-off voltage and/or high channel doping (device type D) devices. The complete set of device characteristics is presented in Table 1. All devices are fabricated with recessed gates, and device types A, C and D have n^+ surface layers.

The nominal performance of these six device types is presented in Table 2. In general R_C is lower with large gate periphery, high channel doping, short gate length and source-to-drain spacings, high pinch off voltage and with an n^+ surface layer. As described previously,[1-3] the conducting state resistance is limited by the FET structure and the conducting path from source-to-drain at zero bias. A value of $R_C W$ varying from 2.2 to 4.8 ohm-mm was obtained in these devices.

The dependence of R_C and C_{NC} on pinch-off voltage (varied principally by channel height variation) is shown in Figure 2 for device types C and D. The advantage of a wider conducting channel in reducing R_C is observed, and the decrease in C_{NC} with increasing channel height is attributed to a reduced sidewall capacitance. For the devices tested, C_{NC}/W values varied from .14 to.27 pF/mm. The switching frequency figure-of-merit (f_{SW}) varied from 190 to 435 GHz for the devices evaluated.

The power handling capacity of these devices in a SPST series switch varies from 1.0 to 2.5 watts as defined by an irreversible change in device parameters. However the devices exhibit a reversible change in resistance at lower power levels, varying from .25 to 1.0 watts as presented in Table 2. The reversible non-linearity is attributed to a peak RF current greater than I_{DSS} in conducting state and a peak RF voltage greater than (V_G-V_P) in the non-conducting state.

Figure 3 illustrates typical non-linear behavior for device type D. The non-linear non-conducting state characteristics can be extended to high power levels by proper gate bias selection $\frac{(V_{BrG}-V_P)}{2}$, namely 6 volts for the FET depicted. For practical purposes this FET has a .25 watts power handling capability in the SPST switch as the strong non-linear behavior between 0.25 and 1.0 watts will not be tolerable in most applications.

Control FET Design

From these results we believe that two conducting states design parameters R_C and $I_{RF\,C}$ (the peak RF current handling capability) are well established as described by Ayasli.[1] Our results support this earlier work. We believe the non-conducting state design parameters C_{NC} and $V_{RF\,NC}$ (the peak RF voltage handling capability) are not as well established. In particular we believe that C_{GS2} and C_{GD2} (Figure 1) are appreciably lower than described by others, as only the sidewall of the gate depletion layer couples to the source and drain contacts above pinch-off. An appreciable contribution to C_{NC} arises from C_{DS}, and the pad and overlap capacitances in multiple finger devices can not be neglected as readily as in amplifier applications where C_{GS} is larger. While we have not isolated individual capacitance components exactly, the approach of Takada et. al.[4] in analyzing capacitance above pinch-off is in qualitative agreement with our results.

The RF voltage handling capability of the devices is larger than originally expected for the submicron gate devices with n^+ surface layer (Device types C and D). The DC gate breakdown voltage V_{brG} shown in Table 2 was measured with source and drain shorted. However voltage handling calculations do not agree well with RF measurements with our present model. Work in this area is continuing.

Conclusions

Based upon these experimental results and our device modeling, we believe FETs with $R_C W$ products of 2.0 ohm-mm and C_{NC}/W values of 0.16 pF/mm are possible, corresponding to f_{SW} figure-of-merit of 500 GHz. For CW power handling requirements of 1 to 2 watt, a reduced f_{SW} of 350 GHz appears feasible. Silicon PIN diodes are capable of higher f_{SW} and appreciable higher power. However, the inherent broadband nature of the MESFET (bias port isolation), the low bias consumption (only leakage current of gate junction in non-conducting state), inherent fast switching time (limited by RC charging through gate isolation resistor) and monolithic circuit compatibility indicate that the MESFET will find increasing usage in control applications whenever high power and/or the most stringent switching figure-of-merit are not required.

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Intrinsic GaAs MESFET Control Device Equivalent Circuit

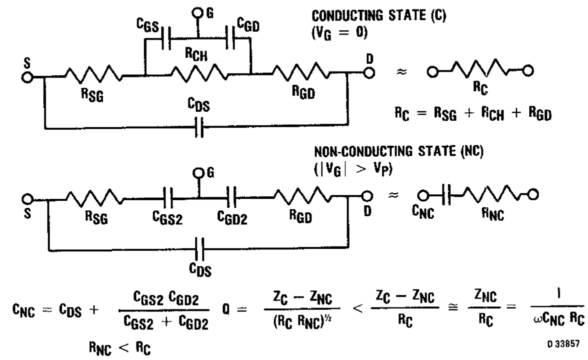


FIGURE 1

R_C and C_{NC} Dependence Upon Pinch-off Voltage for FETs C and D

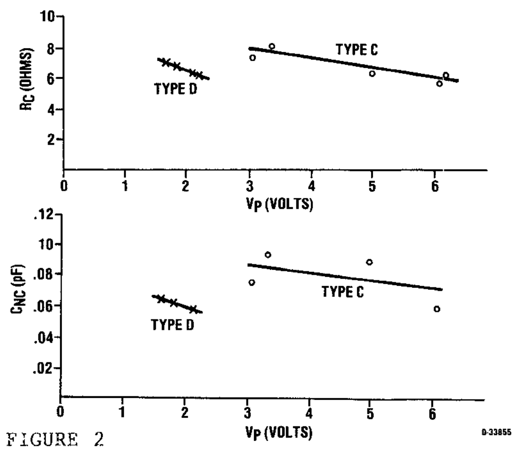
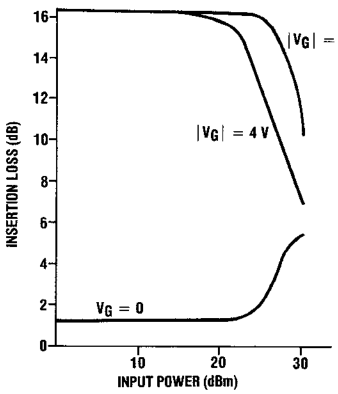


FIGURE 2

Power Handling Capability of Device Type D in SPST Series Switch



NONLINEAR CHARACTERISTICS AT POWER > .25 W
REVERSIBLE CHARACTERISTICS AT POWER < 1 W

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FIGURE 3

GaAs MESFET Control Characteristics

DEVICE TYPE	R_C (OHMS)	C_{NC} (pF)	f_{SW} (GHz)	I_{DSS} (mA)	V_{brG} (V)	P (WATTS)*
A	5.5	0.09	322	100	18	.25/1.5
B	4.0	0.17	234	230	20	1.0/2.5
C	7.5	0.07	303	90	13	0.25/1.0
D	6.1	0.06	435	80	11	0.25/1.0
E	2.6	0.32	191	220	20	1.0/2.5
F	6.6	.084	287	155	20	0.5/1.5

*CW POWER PERFORMANCE IN A SERIES SPST SWITCH (LOWER VALUE CORRESPONDS TO ONSET OF REVERSIBLE NON-LINEAR CHARACTERISTICS WHILE UPPER VALUE IS MAXIMUM POWER HANDLING CAPABILITY).

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TABLE 2

Characteristics of GaAs MESFETs Evaluated

DEVICE TYPE	l_g (μm)	W (μm)	V_P (VOLTS)*	l_{gs} (μm)	l_{gd} (μm)	N_D (cm^{-3})
A	0.8	400	3	1.7	1.7	2×10^{17}
B	1.0	1200	3-5	1.8	2.5	1×10^{17}
C	0.3	400	3-6	1.5	1.5	1.6×10^{17}
D	0.3	400	1.5-2.5	1.4	1.4	3.4×10^{17}
E	1.0	1200	4-5	1.5	1.5	1.1×10^{17}
F	1.0	530	3-4	1.5	1.5	1.2×10^{17}

*RANGE OF PINCH-OFF VOLTAGES TESTED

DEVICES A-D: DISCRETE FETs FABRICATED WITH VAPOR PHASE EPITAXIAL CHANNELS

DEVICES E-F: MONOLITHIC FETs FABRICATED WITH ION IMPLANTED CHANNELS

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TABLE 1